Modification of HDK 20190520

1. **32.768KHz crystal**

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| Target Boards | D3F, D3FP, D3FV, COB |
| Modification | The capacitor for 32.768KHz crystal should be less than 9 pF |
| Description | To avoid the startup issue of 32.768KHz crystal when PMU\_SF is low. The capacitor for 32.768KHz crystal should be less than 9pF to increase the loop gain of crystal circuit. |

Schematic:



1. **PWR\_EN**

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| Target Board | D3F, D3FP, D3FV, COB |
| Modification | Remove the capacitor of PWR\_EN and change the pull up resistor to 100K ohm. |
| Description | There are 2 way to use PWR\_EN pin.   1. PWR\_EN and VBAT rise at the same time. PWR\_EN voltage should follow the VBAT when power on. That’s why the capacitor is removed. 2. PWR\_EN rise after VBAT is ready. In this case, the rise time of VBAT should be less than 500ns.   Therefore, removing the capacitor to increase the rise time of PWR\_EN.  To avoid the bounce of the PWR\_EN, the pull up resistor is change to 100K ohm. |

Schematic:



1. **RST\_N**

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| Target Board | D3F, D3FP, D3FV, COB |
| Modification | Keep the resistor and capacitor of RST\_N |
| Description | The time of VBAT rising to RST\_N rising is 2ms, so we keep pull-up resistor and the capacitor. |

Schematic:



1. **WP and HOLD pins of Flash**

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| Target Board | COB |
| Modification | Remove pull up resistors and pull them up by GPIO |
| Description | To access the flash, Boot rom will read the flash device information to determine if a flash is a single bit or quad bit type. The WP(IO2) and HOLD(IO3) should be high in the beginning.  To support Standard SPI (single bit) only  WP and HOLD pins should keep high when reading SPI flash. But if we have redundant GPIO, we can use it to pull the WP and HOLD pins high and remove both resistors.  Because GPIO16 and GPIO17 are set to output high in the ROM code, GPIO16(as WP) and GPIO17(as HOLD) are recommended for WP and HOLD in Single-bit SPI flash if they are not used for other purpose.  To support Quad SPI only  WP and HOLD becomes to data IO2(GPIO16) and IO3(GPIO17) of QSPI. Pull up resistors are not required. To access the flash, Boot rom determines if a flash is a single bit or quad bit type by reading flash device information in a single bit mode first that is when the two control signals are pulled high if the flash is a quad type  To support both Standard SPI and QSPI  Because WP(IO2) and HOLD(IO3) are connected to GPIO16 and GPIO17, pull-up resistors are not required to in this case. |

Schematic:



1. **Decouple capacitors**

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| Target Board | COB (with external LDO only) |
| Modification | Decide what decouple capacitors can be removed |
| Description | There are decouple capacitors for following power domain: VDD\_RF, EX\_DCDC, VBAT, VDDC. According to below performance test, the capacitor of VBAT, VDDC, EX\_DCDC can be removed. The removing of decouple capacitors for VDD\_RF depends on the requirement of RF performance. If the lower performance is accepted, decouple capacitors for VDD\_RF can be removed, too.  Note: removing decouple capacitors are only for external LDO. |

